

Form PTO-1449 (Modified)	Atty Docket N .: 003692.P007XD3	S rial No.: Not Yet Assign d
List of Patents and Publications Statement (Use several sheets if necessary)	Applicants: Rumennik, V., et al.	
	Filing Date: September 20, 2001 (Concurrently Herewith)	

 11000 U.S. PTO
09/961229


REFERENCE DESIGNATION				U.S. PATENT DOCUMENTS			
Exam. Initial		Date	Document Number	Name	Class	Sub-Class	Filing Dat
SK		10/21/86	4,618,541	Forouhi, et al.			
		12/02/86	4,626,879	Colak			
		05/12/87	4,665,426	Allen, et al.			
		06/28/88	4,754,310	Coe			
		08/16/88	4,764,800	Sander			
		03/07/89	4,811,075	Elkund			
		12/26/89	4,890,146	Williams, et al.			
		05/01/90	4,922,327	Mena, et al.			
		04/23/91	5,010,024	Allen, et al.			
		06/18/91	5,025,296	Fullerton, et al.			
✓		09/08/92	5,146,298	Elkund			

FOREIGN PATENT DOCUMENTS

N .		Document No.	Date	Country	Name	Class	Sub-Class	Trans-lation
SK		DE 43 09 764	09/29/94	Germany				
		57-12557	1/22/82	Japan				
		56-38867	4/14/81	Japan				

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

SK		Appels and Vaes, "High Voltage Thin Layer Devices (RESURF Devices)," IEDM Tech. Digest, pp. 238-241, 1979.
		Fujihira ("Theory of Semiconductor Superjunction Devices," Jpn. J. Appl. Phys., Vol. 36, pp. 6254-6262, Oct. 1997)
✓		Patent Abstract of Japan, Vol. 018, No. 590 (E-1628), 11/10/94 and JP 06224426 (Matsushita Electron Corp.) 08/12/94

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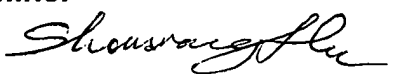
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REFERENCE DESIGNATION				U.S. PATENT DOCUMENTS			
Exam. Initial		Date	Document Number	Name	Class	Sub-Class	Filing Dat
Sle		10/13/92	5,155,574	Yamaguchi			
		08/17/93	5,237,193	Williams, et al.			
		11/02/93	5,258,636	Rumennik, et al.			
		12/14/93	5,270,264	Andideh, et al.			
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		06/28/94	5,324,683	Fitch, et al.			
		09/20/94	5,349,225	Redwine, et al.			
		10/25/94	5,359,221	Miyamoto, et al.			
		01/31/95	5,386,136	Williams, et al.			
		08/01/95	5,438,215	Tihanyi			
✓		05/28/96	5,521,105	Hsu, et al.			

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d	Sle	57-12558	1/22/82	Japan				
s	Sle	6-224426	12/8/94	Japan	Yuji			
b	Sle ✓	JP04107877A	04/09/92	Japan	Yamanishi, Y. et al.			

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)	
Sle	Patent Abstract of Japan, Vol. 016, No. 347 (E-1240), 07/27/92 and JP 04 107867 (Matsushita Electron Corp.) 04/09/92
*	Air-Gap Formation During IMD Deposition to Lower Interconnect Capacitance, B. Shieh, K.C. Saraswat, IEEE Electron Device Letters, Vol., 19, No. 1, January 1998
*	Modeling and Optimization of Lateral High Voltage IC Devices To Minimize 3-D Effects, Hamza Yilmaz, R&D Engineering, Semiconductor Business Division, General Electric Company, NC., pages 290 - 294

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*: Note, these two references are not found.

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SR		08/27/96	5,550,405	Cheung, et al.			
SR		08/05/97	5,654,206	Merrill			
SR		08/12/97	5,656,543	Chung			
SR		08/19/97	5,659,201	Wollesen			
		08/27/96	5,550,405	Cheung, et al.			
		08/05/97	5,654,206	Merrill			
		08/12/97	5,656,543	Chung			
		08/19/97	5,659,201	Wollesen			
SR		08/24/99	5,943,595	Akiyama, et al.			
SR		01/04/00	6,010,926	Rho, et al.			
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